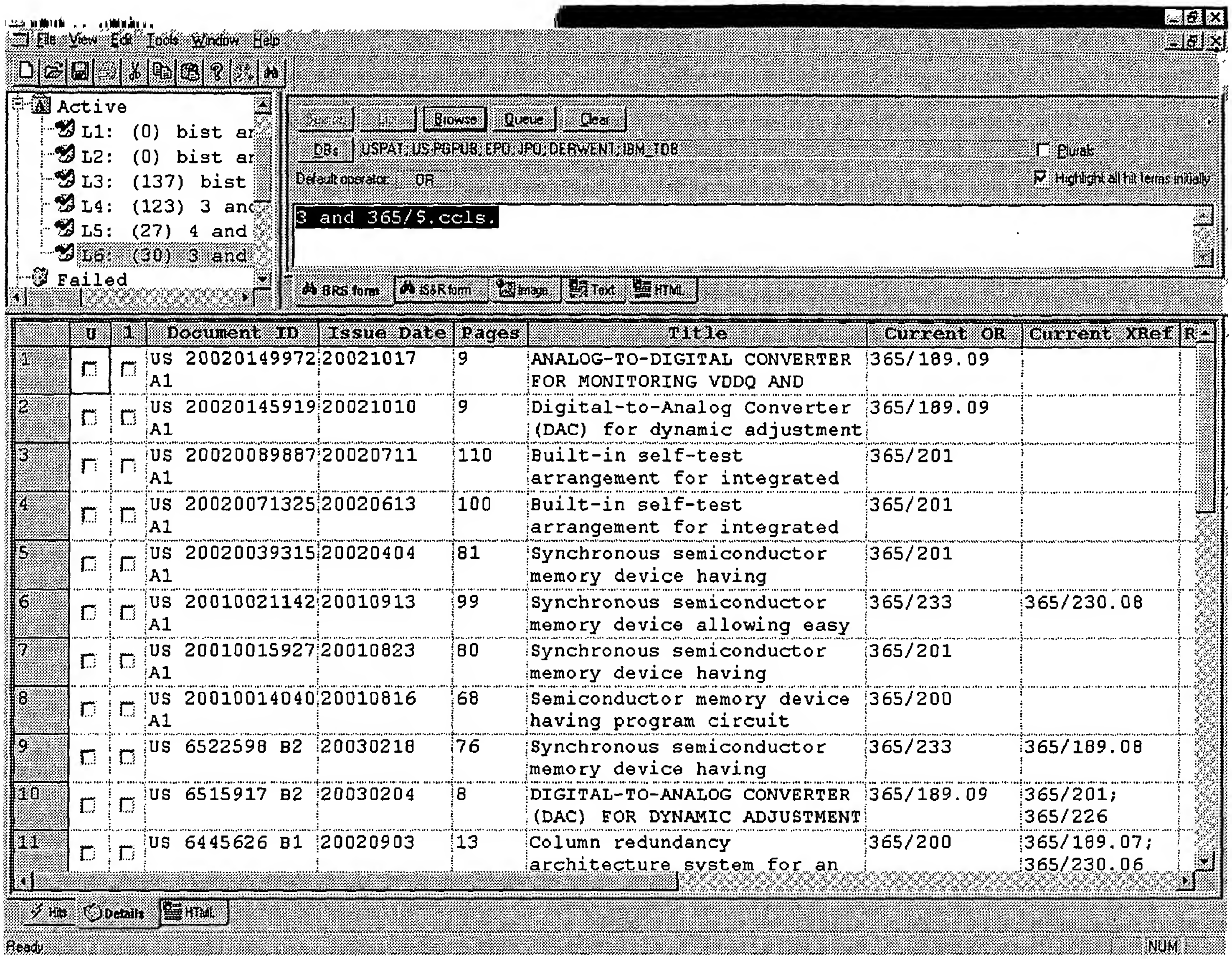


Active
L1: (0) bist ar
L2: (0) bist ar
L3: (137) bist
L4: (123) 3 anc
L5: (27) 4 and
L6: (30) 3 and
Failed

DBs: USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

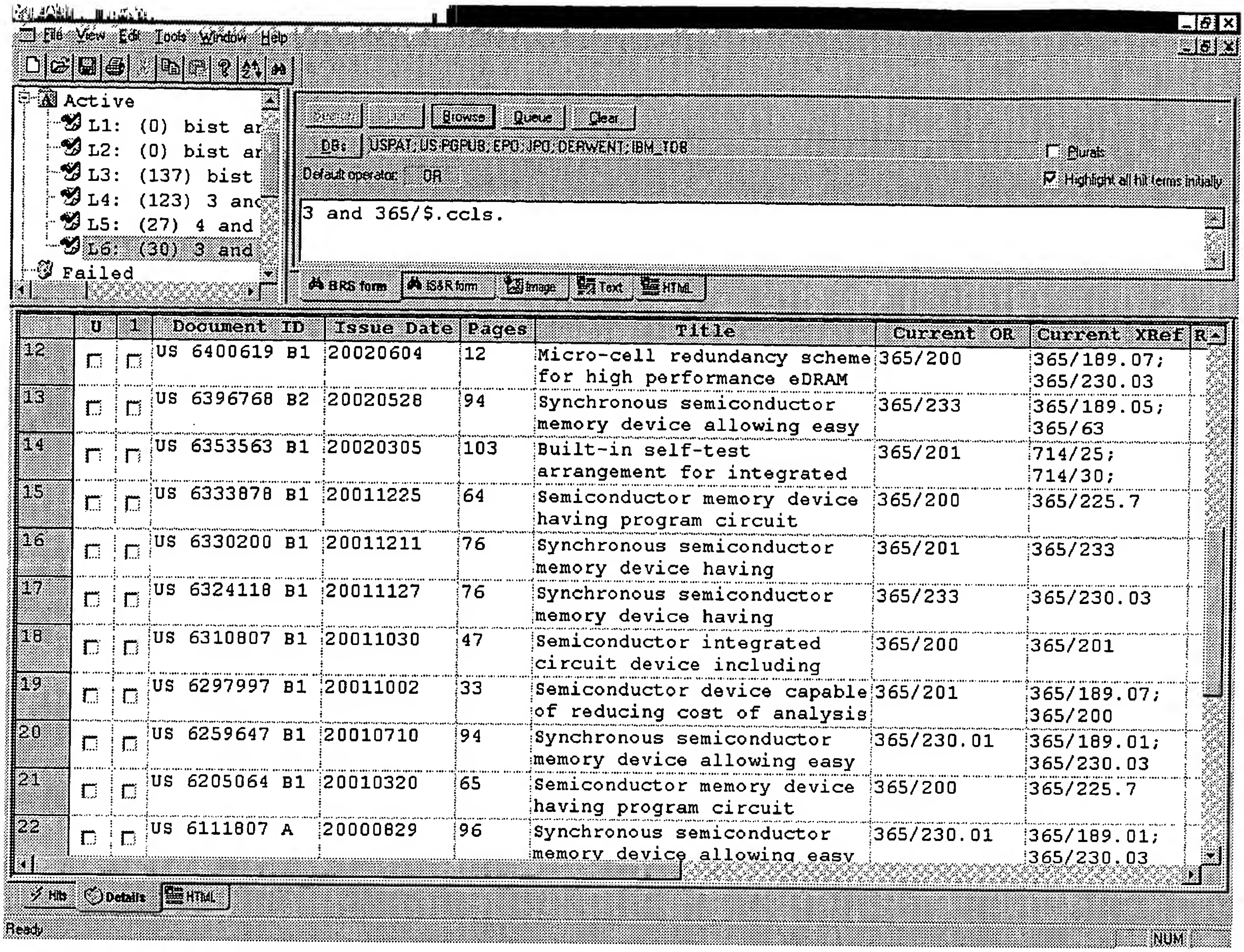
☐ Plurals

☑ Highlight all hit terms initially

Default operator: OR

```
3 and 365/$.ccls.
```

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 20020149972 A1	20021017	9	ANALOG-TO-DIGITAL CONVERTER FOR MONITORING VDDQ AND	365/189.09		
2	☐	☐	US 20020145919 A1	20021010	9	Digital-to-Analog Converter (DAC) for dynamic adjustment	365/189.09		
3	☐	☐	US 20020089887 A1	20020711	110	Built-in self-test arrangement for integrated	365/201		
4	☐	☐	US 20020071325 A1	20020613	100	Built-in self-test arrangement for integrated	365/201		
5	☐	☐	US 20020039315 A1	20020404	81	Synchronous semiconductor memory device having	365/201		
6	☐	☐	US 20010021142 A1	20010913	99	Synchronous semiconductor memory device allowing easy	365/233	365/230.08	
7	☐	☐	US 20010015927 A1	20010823	80	Synchronous semiconductor memory device having	365/201		
8	☐	☐	US 20010014040 A1	20010816	68	Semiconductor memory device having program circuit	365/200		
9	☐	☐	US 6522598 B2	20030218	76	Synchronous semiconductor memory device having	365/233	365/189.08	
10	☐	☐	US 6515917 B2	20030204	8	DIGITAL-TO-ANALOG CONVERTER (DAC) FOR DYNAMIC ADJUSTMENT	365/189.09	365/201; 365/226	
11	☐	☐	US 6445626 B1	20020903	13	Column redundancy architecture system for an	365/200	365/189.07; 365/230.06	



Active
L1: (0) bist ar
L2: (0) bist ar
L3: (137) bist
L4: (123) 3 anc
L5: (27) 4 and
L6: (30) 3 and
Failed

DBs: USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

Default operator: OR

☐ Plurals

☑ Highlight all hit terms initially

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3 and 365/$.ccls.
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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
12	☐	☐	US 6400619 B1	20020604	12	Micro-cell redundancy scheme for high performance eDRAM	365/200	365/189.07; 365/230.03	
13	☐	☐	US 6396768 B2	20020528	94	Synchronous semiconductor memory device allowing easy	365/233	365/189.05; 365/63	
14	☐	☐	US 6353563 B1	20020305	103	Built-in self-test arrangement for integrated	365/201	714/25; 714/30;	
15	☐	☐	US 6333878 B1	20011225	64	Semiconductor memory device having program circuit	365/200	365/225.7	
16	☐	☐	US 6330200 B1	20011211	76	Synchronous semiconductor memory device having	365/201	365/233	
17	☐	☐	US 6324118 B1	20011127	76	Synchronous semiconductor memory device having	365/233	365/230.03	
18	☐	☐	US 6310807 B1	20011030	47	Semiconductor integrated circuit device including	365/200	365/201	
19	☐	☐	US 6297997 B1	20011002	33	Semiconductor device capable of reducing cost of analysis	365/201	365/189.07; 365/200	
20	☐	☐	US 6259647 B1	20010710	94	Synchronous semiconductor memory device allowing easy	365/230.01	365/189.01; 365/230.03	
21	☐	☐	US 6205064 B1	20010320	65	Semiconductor memory device having program circuit	365/200	365/225.7	
22	☐	☐	US 6111807 A	20000829	96	Synchronous semiconductor memory device allowing easy	365/230.01	365/189.01; 365/230.03	

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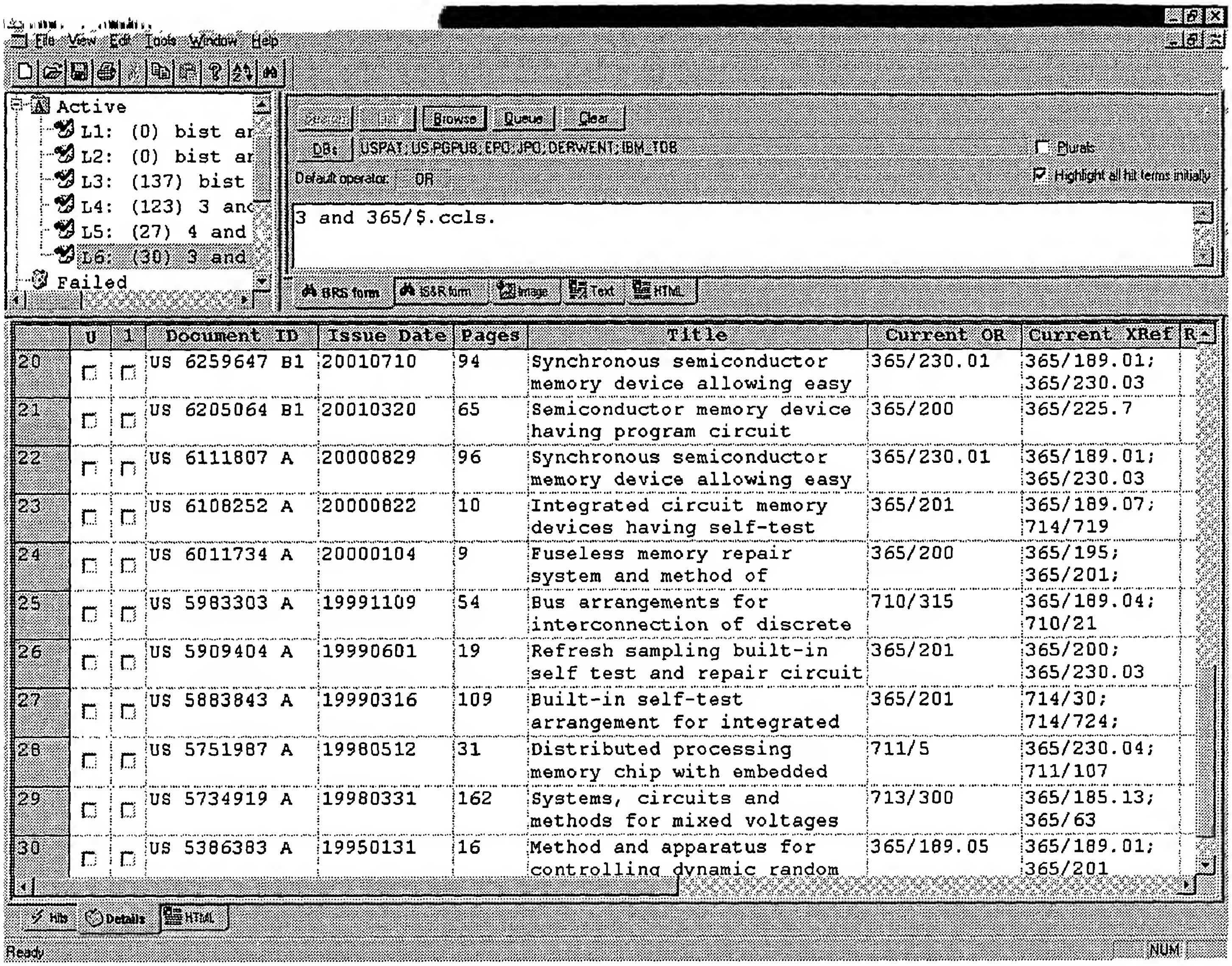
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Active
L1: (0) bist ar
L2: (0) bist ar
L3: (137) bist
L4: (123) 3 anc
L5: (27) 4 and
L6: (30) 3 and
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DBs: USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
20	☐	☐	US 6259647 B1	20010710	94	Synchronous semiconductor memory device allowing easy	365/230.01	365/189.01; 365/230.03	
21	☐	☐	US 6205064 B1	20010320	65	Semiconductor memory device having program circuit	365/200	365/225.7	
22	☐	☐	US 6111807 A	20000829	96	Synchronous semiconductor memory device allowing easy	365/230.01	365/189.01; 365/230.03	
23	☐	☐	US 6108252 A	20000822	10	Integrated circuit memory devices having self-test	365/201	365/189.07; 714/719	
24	☐	☐	US 6011734 A	20000104	9	Fuseless memory repair system and method of	365/200	365/195; 365/201;	
25	☐	☐	US 5983303 A	19991109	54	Bus arrangements for interconnection of discrete	710/315	365/189.04; 710/21	
26	☐	☐	US 5909404 A	19990601	19	Refresh sampling built-in self test and repair circuit	365/201	365/200; 365/230.03	
27	☐	☐	US 5883843 A	19990316	109	Built-in self-test arrangement for integrated	365/201	714/30; 714/724;	
28	☐	☐	US 5751987 A	19980512	31	Distributed processing memory chip with embedded	711/5	365/230.04; 711/107	
29	☐	☐	US 5734919 A	19980331	162	Systems, circuits and methods for mixed voltages	713/300	365/185.13; 365/63	
30	☐	☐	US 5386383 A	19950131	16	Method and apparatus for controlling dynamic random	365/189.05	365/189.01; 365/201	

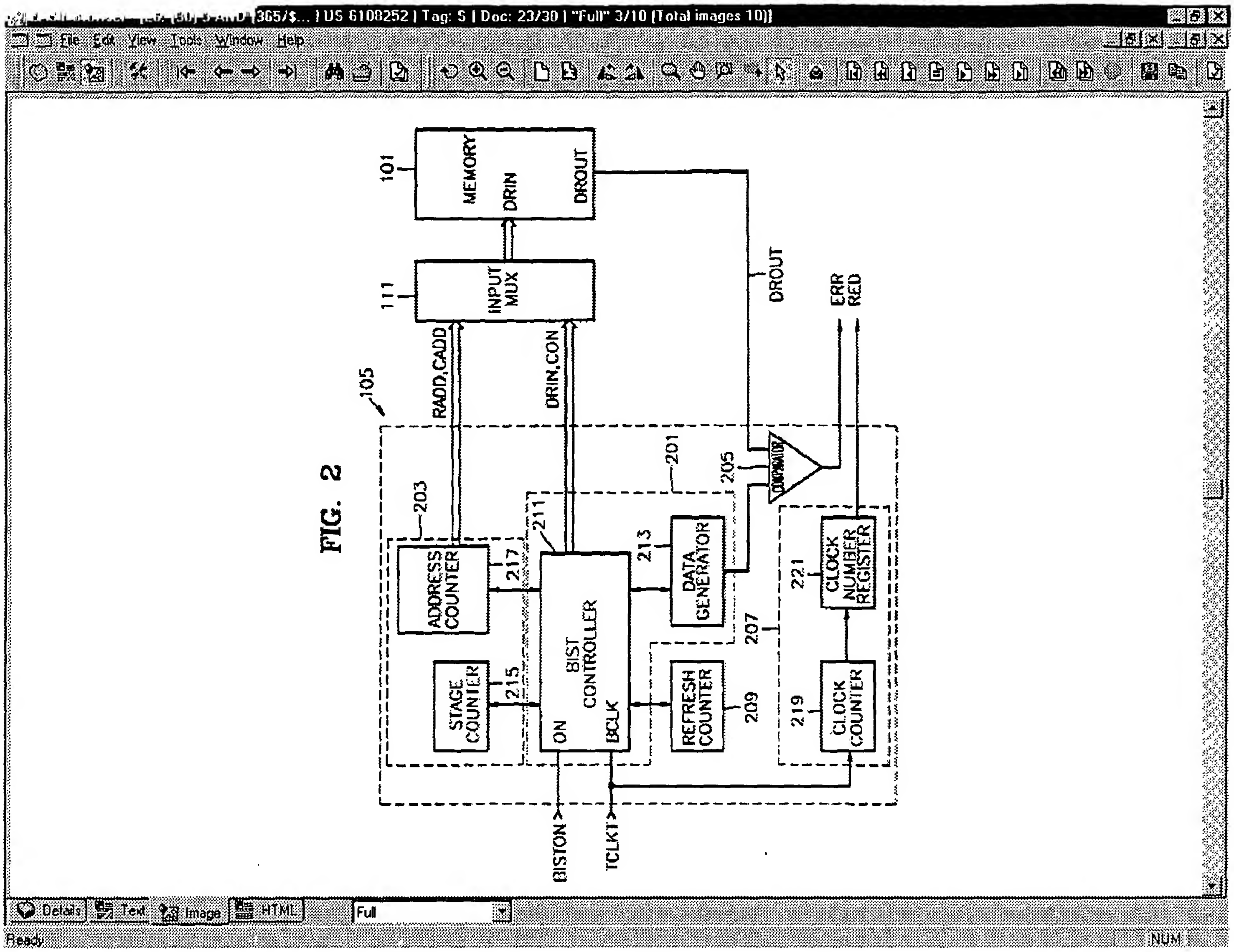
365/$... | US 6108252 | Tag: S | Doc: 23/30 | "Full" 3/10 (Total images 10)

FIG. 2

File
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Tools
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101
MEMORY
DRIN
DROUT
111
INPUT MUX
105
RADD,CADD
DRIN,CON
DROUT
ERR
RED
203
201
205
COMPARATOR
211
213
217
215
ADDRESS COUNTER
STAGE COUNTER
BIST CONTROLLER
ON
BCLK
DATA GENERATOR
REFRESH COUNTER
209
207
221
219
CLOCK NUMBER REGISTER
CLOCK COUNTER
BISTON
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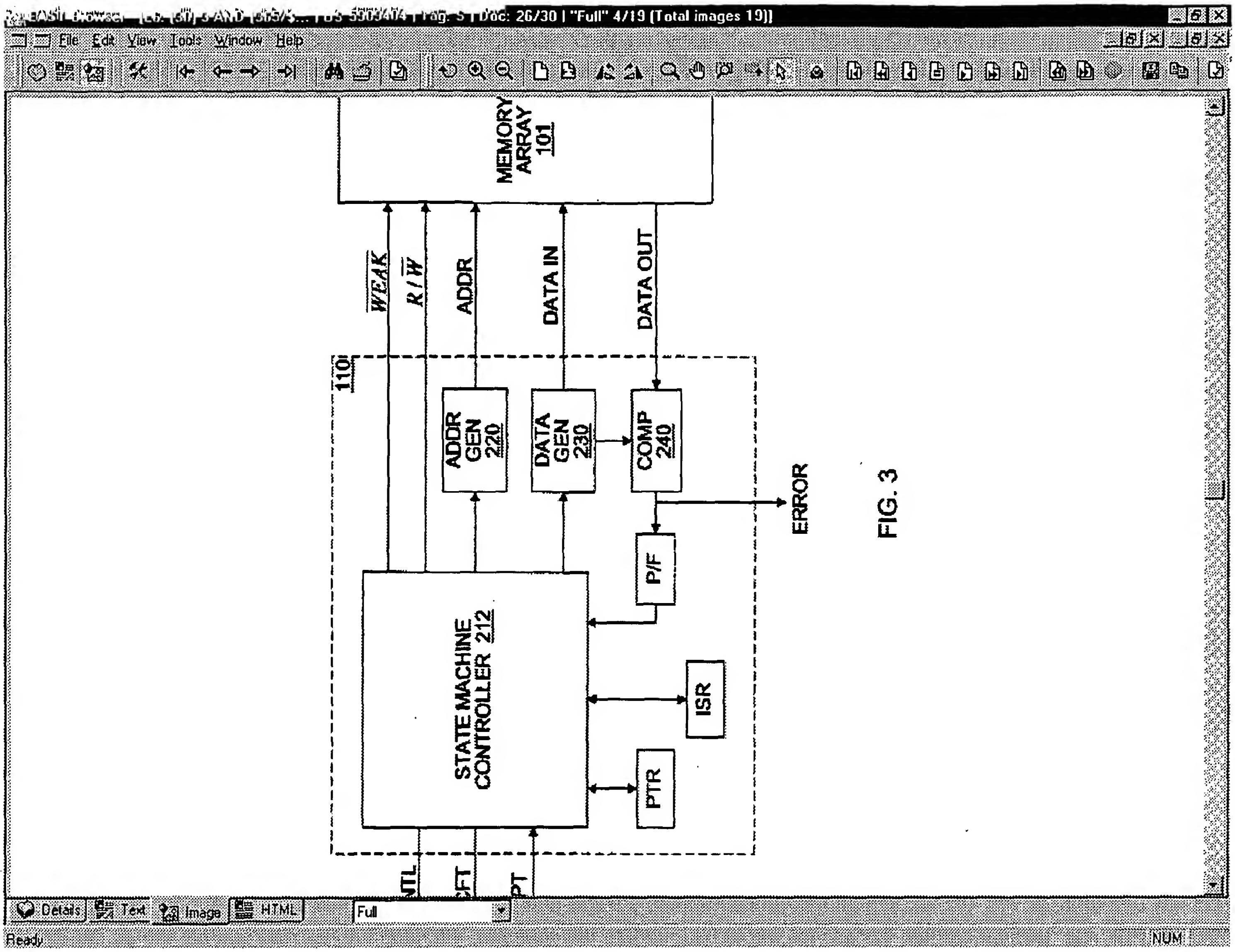
EAST Browser - [L5: (30) 3 AND (365/5... | US 5909404 | Tag: S | Doc: 26/30 | "Full" 4/19 (Total images 19)]
File Edit View Tools Window Help
MEMORY ARRAY 101
WEAK
R / W
ADDR
DATA IN
DATA OUT
110
ADDR GEN 220
DATA GEN 230
COMP 240
ERROR
P/F
STATE MACHINE CONTROLLER 212
ISR
PTR
NTL
CFT
PT
Details
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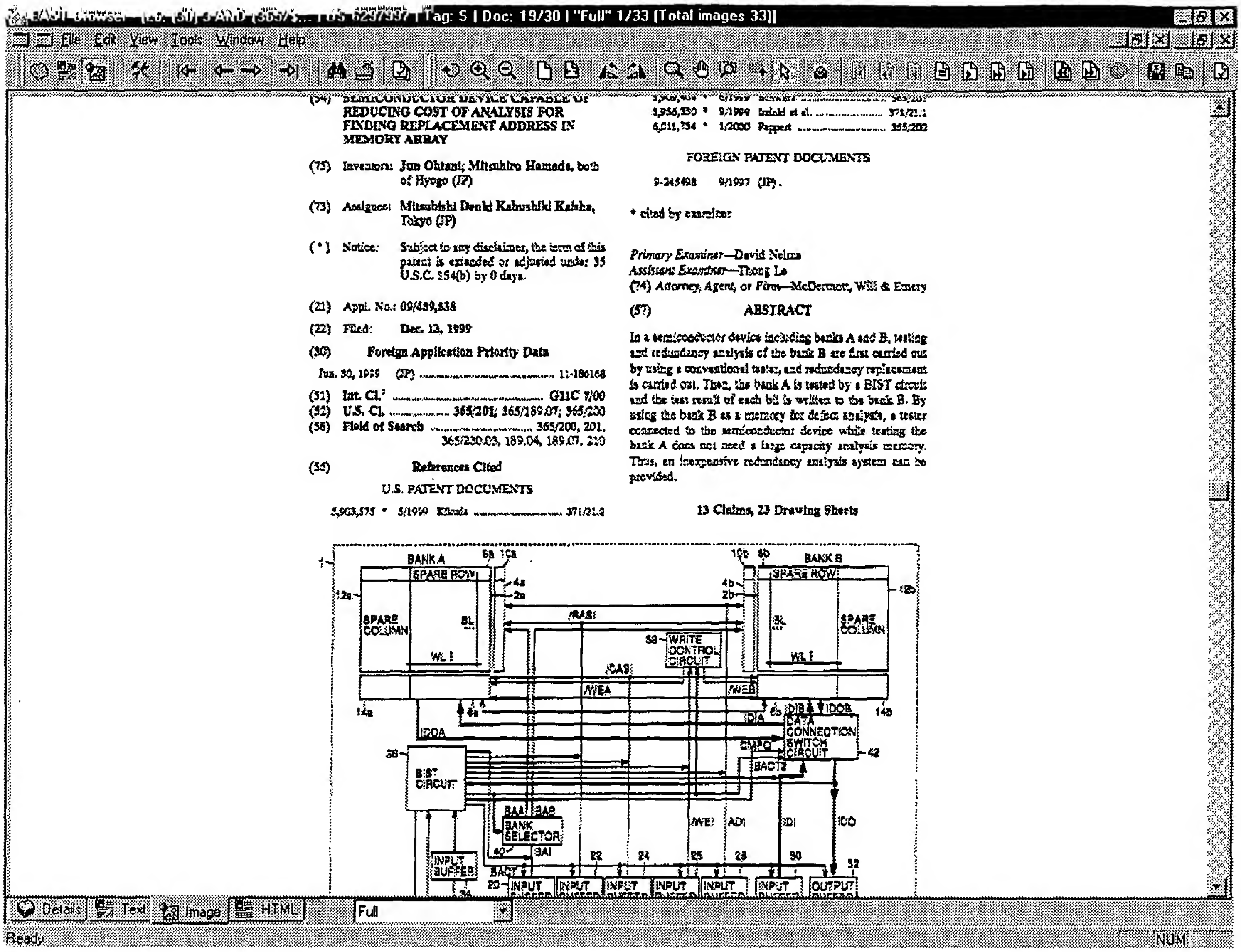
Full

FIG. 3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File
Edit
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Tools
Window
Help
BANK A
BANK B
SPARE ROW
SPARE COLUMN
BL
WL
/RAS
/CAS
/WEA
/WEB
WRITE CONTROL CIRCUIT
DATA CONNECTION SWITCH CIRCUIT
BIST CIRCUIT
BANK SELECTOR
INPUT BUFFER
OUTPUT BUFFER
IDOA
IDIA
DIB
IDOB
CMPO
BACT2
BAA
BAB
BAI
BACT
/WEI
ADI
DI
DO
1
2a
2b
4a
4b
6a
6b
10a
10b
12a
12b
14a
14b
20
22
24
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42
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(54) SEMICONDUCTOR DEVICE CAPABLE OF REDUCING COST OF ANALYSIS FOR FINDING REPLACEMENT ADDRESS IN MEMORY ARRAY

(75) Inventors: Jun Ohtani; Mitsuhiro Hamada, both of Hyogo (JP)

(73) Assignee: Mitsubishi Denki Kabushiki Kaisha, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/459,538

(22) Filed: Dec. 13, 1999

(30) Foreign Application Priority Data

Jun. 30, 1999 (JP) 11-186168

(51) Int. Cl.^{7} G11C 7/00
(52) U.S. Cl. 365/201; 365/189.07; 365/200
(58) Field of Search 365/200, 201, 365/230.03, 189.04, 189.07, 230

(56) References Cited

U.S. PATENT DOCUMENTS

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5,956,350 * 9/1999 Irrinki et al. 371/21.1
6,011,734 * 1/2000 Pappert 365/200

FOREIGN PATENT DOCUMENTS

9-245498 9/1997 (JP).

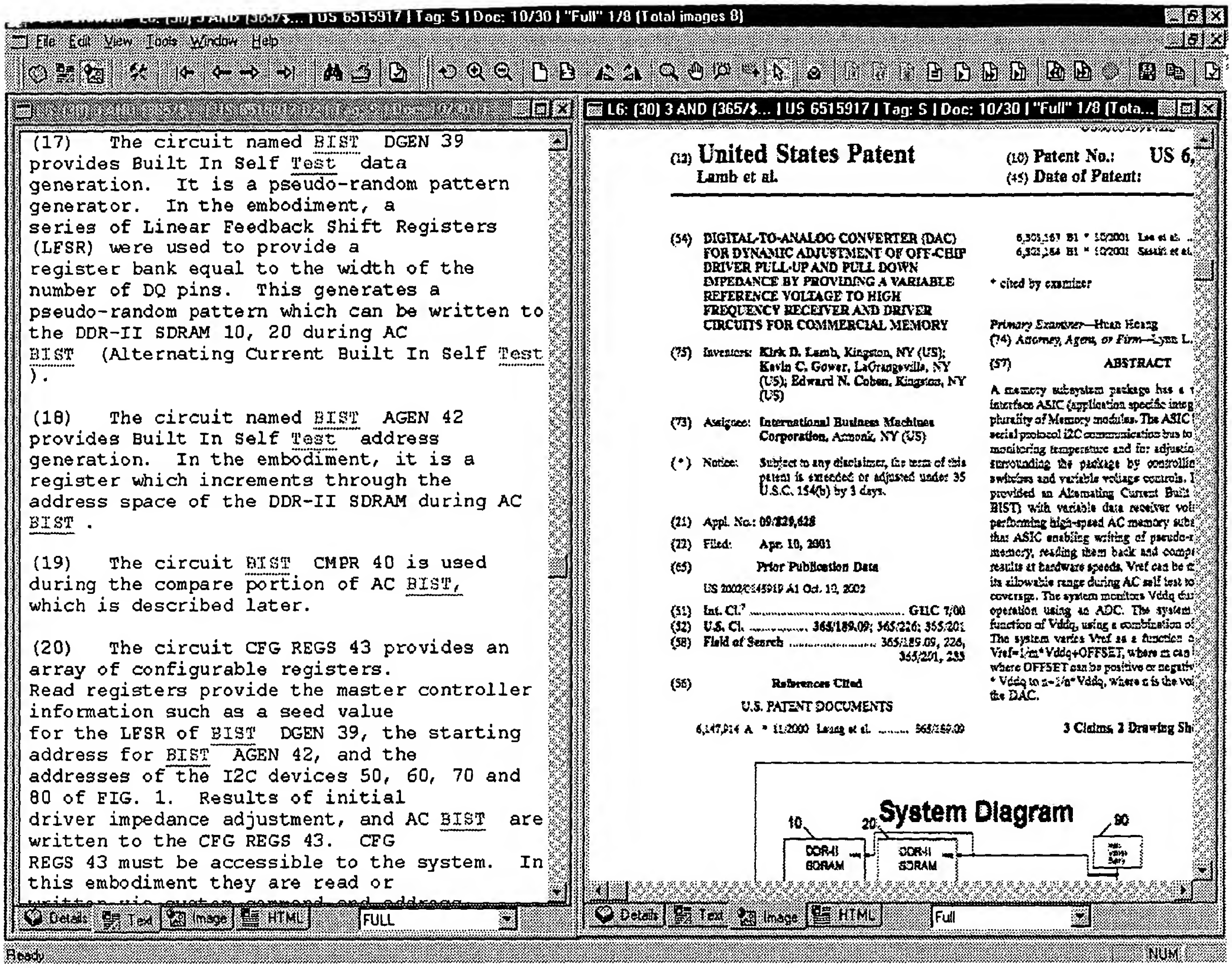
* cited by examiner

Primary Examiner—David Nelms
Assistant Examiner—Thong Le
(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57) ABSTRACT

In a semiconductor device including banks A and B, testing and redundancy analysis of the bank B are first carried out by using a conventional tester, and redundancy replacement is carried out. Then, the bank A is tested by a BIST circuit and the test result of each bit is written to the bank B. By using the bank B as a memory for defect analysis, a tester connected to the semiconductor device while testing the bank A does not need a large capacity analysis memory. Thus, an inexpensive redundancy analysis system can be provided.

13 Claims, 23 Drawing Sheets


L6: (30) 3 AND (365/$... | US 6515917 | Tag: S | Doc: 10/30 | "Full" 1/8 (Total images 8)
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(17) The circuit named BIST DGEN 39 provides Built In Self Test data generation. It is a pseudo-random pattern generator. In the embodiment, a series of Linear Feedback Shift Registers (LFSR) were used to provide a register bank equal to the width of the number of DQ pins. This generates a pseudo-random pattern which can be written to the DDR-II SDRAM 10, 20 during AC BIST (Alternating Current Built In Self Test).

(18) The circuit named BIST AGEN 42 provides Built In Self Test address generation. In the embodiment, it is a register which increments through the address space of the DDR-II SDRAM during AC BIST .

(19) The circuit BIST CMPR 40 is used during the compare portion of AC BIST, which is described later.

(20) The circuit CFG REGS 43 provides an array of configurable registers. Read registers provide the master controller information such as a seed value for the LFSR of BIST DGEN 39, the starting address for BIST AGEN 42, and the addresses of the I2C devices 50, 60, 70 and 80 of FIG. 1. Results of initial driver impedance adjustment, and AC BIST are written to the CFG REGS 43. CFG REGS 43 must be accessible to the system. In this embodiment they are read or

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(12) **United States Patent**
Lamb et al.

(10) **Patent No.:** US 6,
(45) **Date of Patent:**

(54) **DIGITAL-TO-ANALOG CONVERTER (DAC) FOR DYNAMIC ADJUSTMENT OF OFF-CHIP DRIVER PULL-UP AND PULL DOWN IMPEDANCE BY PROVIDING A VARIABLE REFERENCE VOLTAGE TO HIGH FREQUENCY RECEIVER AND DRIVER CIRCUITS FOR COMMERCIAL MEMORY**

(75) Inventors: **Kirk D. Lamb**, Kingston, NY (US); **Kevin C. Gower**, LaGrangeville, NY (US); **Edward N. Cohen**, Kingston, NY (US)

(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 3 days.

(21) Appl. No.: **09/829,628**

(22) Filed: **Apr. 10, 2001**

(65) **Prior Publication Data**

US 2002/0145919 A1 Oct. 10, 2002

(51) **Int. Cl.**^{7} **G11C 7/00**
(52) **U.S. Cl.** **365/189.09; 365/226; 365/201**
(58) **Field of Search** 365/189.09, 226, 365/201, 233

(56) **References Cited**

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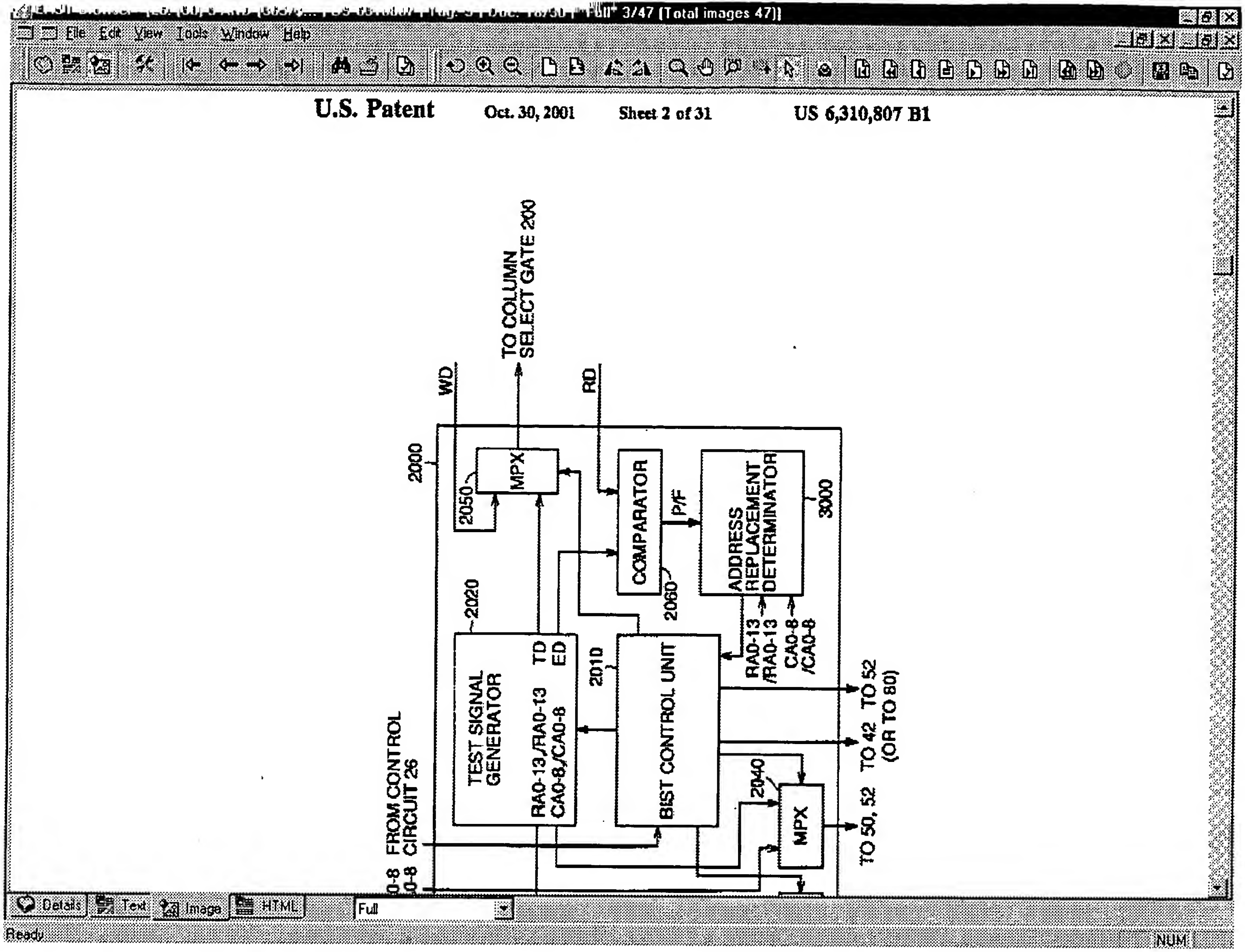
* cited by examiner

Primary Examiner—Huan Hoang
(74) *Attorney, Agent, or Firm*—Lynn L.

(57) **ABSTRACT**

A memory subsystem package has a
interface ASIC (application specific integ
plurality of Memory modules. The ASIC
serial protocol I2C communication bus to
monitoring temperature and for adjustin
surrounding the package by controllin
switches and variable voltage controls. I
provided an Alternating Current Built
BIST) with variable data receiver vol
performing high-speed AC memory subs
that ASIC enabling writing of pseudo-r
memory, reading them back and compa
results at hardware speeds. Vref can be
its allowable range during AC self test to
coverage. The system monitors Vddq du
operation using an ADC. The system
function of Vddq, using a combination of
The system varies Vref as a function o
Vref=1/m*Vddq+OFFSET, where m can
where OFFSET can be positive or negativ
* Vddq to n=1/n*Vddq, where n is the vo
the DAC.

3 Claims, 2 Drawing Sh



3/47 (Total images 47)
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U.S. Patent Oct. 30, 2001 Sheet 2 of 31 US 6,310,807 B1

WD
TO COLUMN SELECT GATE 200
RD
2000
2050
MPX
COMPARATOR
P/F
ADDRESS REPLACEMENT DETERMINATOR
3000
2060
2020
TEST SIGNAL GENERATOR
RA0-13,/RA0-13
CA0-8,/CA0-8
TD
ED
2010
BIST CONTROL UNIT
RA0-13
/RA0-13
CA0-8
/CA0-8
TO 52
TO 42
(OR TO 80)
2040
MPX
TO 50, 52
FROM CONTROL CIRCUIT 26
0-8
0-8